Attorney's Docket No.:

77/182002/US3413D1

THE UNITED STATES PATENT AND TRADEMARK OFFICE

Art Unit:

2823

Serial No.: 09/635,832

Applicant : Yamazaki, et al.

Examiner:

Fernando Toled

Filed

: August 9, 2000

Title

: SEMICONDUCTOR DEVICE AND MANUFACTURING METHOD

THEREFOR

ommissioner for Paten. ashington, D.C. 20231

REPLY TO NOTICE OF NON-COMPLIA...

In response to the Notice dated March 20, 2002 in above-identified application, please find below the entire complete address and the state of th

Please elect Group II, claims 18-37 and 39-40.

Please amend claim 18-20, 23, 25, and 28-37 as follows:

18. (Amended) An integrated circuit comprising: a CMOS circuit;

CERTIFICATE OF MAILING BY FIRST CLASS MAIL

I hereby certify under 37 CFR §1.8(a) that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage on the date indicated below and is addressed to the Commissioner for Patents, Washington, D.C. 20231.

April 2, 2002

Date of Deposit

Signature

Susan Regan

Typed or Printed Name of Person Signing Certificate